Substitute Form PTO-1449 (Modified) U.S. Department of Commerce Patent and Trademark Office

Attorney's Docket No. 10559-487001

Application No. 09/966,349

winformation Disclosure Statement by Applicant (Use several sheets if necessary)

Applicant Donald F. Hooper, et al.

Filing Date September 28, 2001 Group Art Unit 2664

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	JW	WO 03/030461	4/10/2003	WIPO				
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V	JY	WO 97/38372	10/16/1997	WIPO				

X*= An English language abstract is provided.

	Other D	ocuments (include Author, Title, Date, and Place of Publication)
Examiner Initial	Desig. ID	Document
KM	JZ	"10-/100-Mbps Ethernet Media Access Controller (MAC) Core"; NEC Electronics Inc., pp. 1-5, (December 1998).
	KA	Beckerle, M.J., "Overview of the START (*T) multithreaded computer" Compcon Spring '93, Digest of Papers, 22-26 February 1993, San Francisco, California, pp. 148-156 (1993), (abstract only)
	KB	Byrd et al., "Multithread Processor Architectures," IEEE Spectrum, 32(8): 38-46, (August 1995).
	KC	Chandranmenon, G.P. et al., "Trading Packet Headers for Packet Processing," IEEE/ACM Transactions on Networking 4(2): 141-152 (April 1996)
V	KD	Dictionary of Computer Words: An A to Z Guide to Today's Computers, Revised Edition, Houghton Mifflin Company: Boston, Massachusetts, pp. 220, (1995)

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EXAMINER: Initials citation considered. Draw line through citation if no next communication to applicant.	t in conformance and not considered. Include copy of this form with

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-487001	Application No. 09/966,349
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Donald F. Hooper, et al.	
		Filing Date September 28, 2001	Group Art Unit 2664

	Other D	ocuments (include Author, Title, Date, and Place of Publication)
Examiner	Desig.	
Initial	ID	Document
KM	KE	Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller, Hardware Reference Manual, Digital Equipment Corporation, pages i-x, 1-1 through 1-5, 2-1 through 2-12, 3-1 through 3-38, 4-31 through 5-2, 6-1 through 6-24, (March 1998)
	KF	Doyle et al. (Eds.), Microsoft Press Computer Dictionary, 2 nd ed., Microsoft Press: Redmond: Washington, USA, pp. 326, (1994)
	KG	English language abstract of Japanese Patent Application JP59111533, published 06/27/84, entitled: "Digital Data Arithmetic Circuit".
	KH	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, pp. 146-156, (1995)
	KI	Frazier, H., "Gigabit Ethernet: From 100 to 1,000 Mbps", IEEE Internet Computing, pp. 24-31, (January/February 1999).
	KJ	Frazier, H., "The 802.3z Gigabit Ethernet Standard", IEEE Network, pp. 6-7, (May/June 1998)
	KK	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, 40(1):103-117, (1997).
	KL	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 2 pages, (1998).
	KM	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, pp. 12-21, (1997).
	KN	Hyde, R.L., "Overview of Memory Management," Byte, 13(4):219-225, (1998)
	ко	Ippoliti, et al., "Parallel Media Access Controller for Packet Communications at Gb/s Rates", ICC/Supercom'90, Atlanta, Georgia, April 15, 1990, IEEE, pp. 991-996 (1990)
	KP	Jenks, G. and J.L. Gaudiot, "Nomadic Threads: A migrating multithread approach to remote memory accesses in multiprocessors", Proceedings of the 1996 Conference on Parallel Architecture and Compilation Techniques, 20-23 October 1996, Boston, Massachusetts, (abstract only).
	KQ	Litch, T. and J. Slaton, "StrongARMing Portable Communications," IEEE Micro, pp. 48-55 (March/April 1998)
	KR	News.Com, August 26, 1999. "Enterprise Hardware, Intel Expected to Unveil New Networking Chip," http://new.com.com/Intel+expected+to+unveil+new+networking+chip/2100-1001 3-230315.html (accessed on 08/23/05), pages 1-5
	KS	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," http://www.cs.wustl.edu/~schmidt/PDF/JPDC-96.pdf#search='The%20Performance%20of%20Alternative%20Threading%20Architectures%20for%20Parallel%20Communication%20Subsystems 13 November 1998., pp. 1-19
	KT	Thistle et al., "A Processor Architecture for Horizon," Proceedings Supercomputing '88, IEEE Computer Society, 14-18 November 1988, Orlando, Florida, pp. 35-41 (1988)
	KU	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, pp. 191-201 (1995)
	ΚV	Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, pp. 22-28, (1998)
V	KW	Turner et al., "Design of a High Performance Active Router," Washington University in Saint Louis, Applied Research Lab, Online Internet Document, 18 March 1999 (20 pages)

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/Kev:	in Mew/	04/27/2006
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(Other Documents (include Author, Title, Date, and Place of Publication)			
Examiner Initial	Desig. ID	Document		
KM	кх	Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-369.		
KM	KY	Wazlowski et al., "PRISM-II computer and architecture," IEEE Workshop on FPGAs for Custom Computing Machines, pp. 9-16, (1993)		

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